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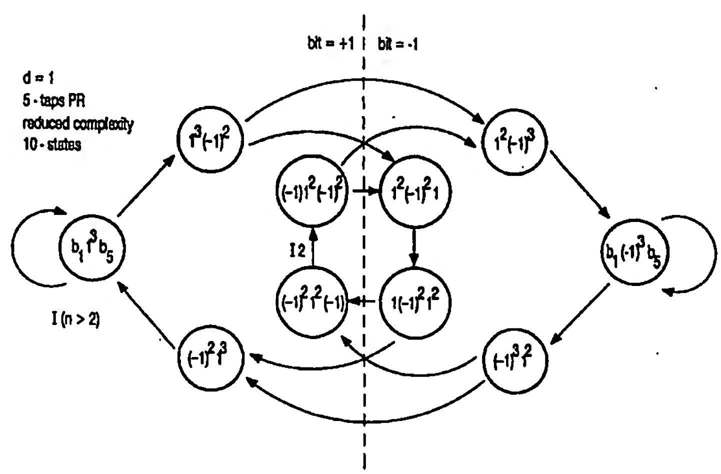

(57) Abstract

A partial response maximum likelihood (PRML) bit detection apparatus is disclosed for deriving a bit sequence from an input information signal. The apparatus comprises input means for receiving the input information signal, sampling means for sampling the input information signal at sampling instants so as to obtain samples of the input information signal at said sampling instants, conversion means for converting an array of said samples into an array of bits of a first or a second binary value, detection means for repeatedly detecting a state for subsequent sequences of n subsequent bits of said array of bits, said subsequent sequences being obtained by shifting a time window of n subsequent bits each time over one bit in time, means for establishing the best path through the states, and deriving means for deriving a sequence of bits in accordance with the best path through said states. In accordance with the invention, n is larger than 3, and sequences of n subsequent bits having n–1 directly successive bits of the same binary value are allocated to the same state. In a specific embodiment is n an odd number larger than 4. Now, sequences of n subsequent bits having n–2 directly successive bits of the same binary value as the central n–2 bits in such n–bit sequence, are allocated to the same state. This results in an a PRML detection apparatus with reduced complexity.

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Partial response maximum likelihood (PRML) bit detection apparatus.

The invention relates to a partial response maximum likelihood (PRML) bit detection apparatus for deriving a bit sequence from an input information signal, comprises

- input means (1) for receiving the input information signal,
- sampling means for sampling, at a predetermined sampling frequency, the input information signal at sampling instants t_i so as to obtain sample values of the input information signal at said sampling instants t_i, said sampling frequency having a relationship with a bit frequency,
- calculation means for

(a) calculating at a sampling instant t_i for each of a plurality of states s_j at said sampling instant, an optimum path metric value $PM(s_j,t_i)$ and for determining for each of the plurality of states a best predecessor state at the directly preceding sampling instant t_{i-1}, a state at said sampling instant identifying a sequence of n subsequent bits,

(b) establishing the best path from the state at the said sampling instant t_i having the lowest optimum path metric value, back in time towards the sampling instant t_{i-N} via best predecessor states, established earlier for earlier sampling instants, to establish an optimum state at said sampling instant t_{i-N},

(c) outputting at least one bit of said n bits of the sequence of bits corresponding to said established optimum state at said sampling instant t_{i-N},

(d) repeating said steps (a) to (c) for a subsequent sampling instant t_{i+1}.

The PRML bit detection apparatus is based on a finite state machine with states corresponding to specific n-bit sequences.

Earlier filed EP patent application no. 98203146.0, having a filing date of 18.09.98 (PHN 17088), describes an apparatus for deriving amplitude values for such PRML bit detection apparatus. The amplitudes are derived from an input information signal, which amplitude values can be used as reference levels for the states of a finite state machine, which are needed for the computation of the likelihood functional in the said partial response maximum likelihood (PRML) bit detection apparatus.

PRML detection requires reference amplitude-levels for each state in the corresponding finite-state-machine (FSM), from which the likelihood of different paths is computed, given the sampled signal waveform. The well known Viterbi-algorithm enables very efficient computation of the most likely path. Each state of an n-taps partial response (PR) corresponds with one of the possible n-bits environments as shown e.g. in Figures 1 and 2. In standard PRML detection, an equalizer setting is chosen so that a simple symmetrical partial response is realized in the nominal situation of zero tilt of the disc with respect to the laser beam, i.e. with simple integer-valued coefficients. That single equalizer may not be optimal in terms of timing recovery. In such case a solution with two equalizers can be implemented, with one equalizer for the timing recovery, and a second one to equalize to the partial response levels. The second one may be made adaptive so that channel fluctuations may be followed, if a robust control mechanism can be set-up, e.g. one that measures the obliqueness of the channel, eg. from the eye-pattern, and transforms this into an adaptation of the tap-values of the equalizer. Non-linearities such as a systematic asymmetry between marks and non-marks (which can be runlenght dependent) are also a problem to be dealt with and are not accounted for in standard PRML using a linear partial response.

The invention aims at providing an improved PRML bit detection apparatus, which has a lower complexity.

In accordance with the invention, the apparatus for deriving a bit sequence from an input information signal, comprises

- input means (1) for receiving the input information signal,
- sampling means for sampling, at a predetermined sampling frequency, the input information signal at sampling instants t_i so as to obtain sample values of the input information signal at said sampling instants t_i, said sampling frequency having a relationship with a bit frequency,
- calculation means for

(a) calculating at a sampling instant t_i for each of a plurality of states s_j at said sampling instant, an optimum path metric value $PM(s_j,t_i)$ and for determining for each of the plurality of states a best predecessor state at the directly preceding sampling instant t_{i-1}, a state at said sampling instant identifying a sequence of n subsequent bits,

(b) establishing the best path from the state at the said sampling instant t_i having the lowest optimum path metric value, back in time towards the sampling instant t_{i-N} via best predecessor states, established earlier for earlier sampling instants, to establish an optimum state at said sampling instant t_{i-N},

(c) outputting at least one bit of said n bits of the sequence of bits corresponding to said established optimum state at said sampling instant t_{i-N},

(d) repeating said steps (a) to (c) for a subsequent sampling instant t_{i+1},

characterized in that n is larger than 3, and that sequences of n subsequent bits having n-1 directly successive bits of the same binary value are allocated to the same state, and in another aspect of the invention, the for deriving a bit sequence from an input information signal, comprises

- input means (1) for receiving the input information signal,
- sampling means for sampling, at a predetermined sampling frequency, the input information signal at sampling instants t_i so as to obtain sample values of the input information signal at said sampling instants t_i, said sampling frequency having a relationship with a bit frequency,
- calculation means for

(a) calculating at a sampling instant t_i for each of a plurality of states s_j at said sampling instant, an optimum path metric value $PM(s_j,t_i)$ and for determining for each of the plurality of states a best predecessor state at the directly preceding sampling instant t_{i-1}, a state at said sampling instant identifying a sequence of n subsequent bits,

(b) establishing the best path from the state at the said sampling instant t_i having the lowest optimum path metric value, back in time towards the sampling instant t_{i-N} via best predecessor states, established earlier for earlier sampling instants, to establish an optimum state at said sampling instant t_{i-N},

(c) outputting at least one bit of said n bits of the sequence of bits corresponding to said established optimum state at said sampling instant t_{i-N},

repeating said steps (a) to (c) for a subsequent sampling instant t_{i+1},

characterized in that said calculation means is adapted to obtain said optimum path metric value for said state at said sampling instant t_i in step (a) by

(a1) comparing the optimum path metric values of all possible predecessor states at the directly preceding instant t_{i-1} of the said state at the instant t_i,

(a2) select the predecessor state at the directly preceding instant t_{i-1} having the smallest optimum path metric value as said best predecessor state,

(a3) combining the optimum path metric value of the best predecessor state at said directly preceding sampling instant t_{i-1} and a branch metric value corresponding to said state at said instant t_i, so as to obtain said optimum path metric value for said state, said branch metric value for said state being obtained from the sample value at said sampling instant and a reference amplitude, which reference amplitude has a relationship with said state.

The invention is based on the following recognition. With the apparatus in accordance with the invention as claimed in claim 1, the number of states have been decreased significantly. This results in a reduced complexity in the calculation for finding the most likely path in the corresponding finite state machine. With the apparatus in accordance with claim 6, the complexity is also reduced, for the reason that the add-compare-select strategy normally carried out in PRML detection systems has been replaced by a simpler compare-select-add strategy.

These and other aspects of the invention will become apparent from and will be elucidated further in the following figure description, in which

figure 1 shows a finite-state diagram of a 3-taps state detector for a d=1 channel code,

figure 2 shows a finite-state diagram of a 5-taps state detector for a d=1 channel code,

figure 3 shows the bit-error-rate (BER) as function of tangential disc tilt for phase-change recording, for 3-taps and 5-taps PRML, for Full-Response ML (FRML), also known as 'runlength push-back detection', and for Threshold Detection (TD),

figure 4 shows a finite-state diagram of a 5-taps PRML state detector with reduced complexity for a d=1 channel code,

figure 5 shows the bit-error-rate (BER) as function of tangential disc tilt for phase-change recording, for 5-taps and 5-taps reduced-complexity (r.c.) PRML, for Full-Response ML (FRML), and for Threshold Detection (TD),

figure 6 shows the retrieved amplitudes for 5-taps PRML, as function of tangential tilt.

figure 7 shows the technique of PRML detection,

figure 8 shows again the finite state diagram of a 3-taps state detector for

a d=1 channel code and the trellis diagram for this detector,

figure 9 the various paths through the states,

figure 10 shows in figure 10a a finite-state diagram of a 5-taps state detector for a d=3 channel code and in figure 10b the corresponding finite-state diagram of the 5-taps PRML state detector of figure 10a with reduced complexity,

figure 11 shows in figure 11a a finite-state diagram of a 7-taps state detector for a d=3 channel code and in figure 11b the corresponding finite-state diagram of the 7-taps PRML state detector of figure 11a with reduced complexity, and

figure 12 shows an embodiment of the PRML apparatus.

A PRML bit detection apparatus with reduced complexity will be described. Partial-Response Maximum-Likelihood (PRML) detection is a candidate to replace the standard technique of Threshold Detection (TD) as used in CD and DVD-like systems. For the new DVR (digital video recorder) system, which is an optical recording/reproduction system, where a d=1 channel code is used, a 3-taps PRML detector has been proposed. Investigations have shown that an increase in the number of taps yields a markedly improved performance in terms of the bit-error-rate (BER). However, this implies also an increase in complexity of the Viterbi-trellis, which is linearly dependent on the number of states in the finite-state-machine (FSM) that is used for a n+1-taps PRML. The number of states N_s amounts to 2 times $N_{d=1}(n)$ with $N_{d=1}(n)$ the Fibonacci numbers, i.e. the number of sequences of length n for a d=1 constraint.

The number N_s of states and the number N_B of the branches connecting the states in the trellis diagram are shown in Table 1 for some choices of the number of taps. The main drawback of using a 5-taps PRML is its largely increased complexity (+167%) compared to a 3-taps PRML.

number of taps	N_s	N_B
3	6	10
5-r.c.	10	16
5	16	26

Table 1: Number of states (N_s) and number of branches (N_B) of the Finite-State-Machine (FSM) as a function of the number of taps of the PRML detector (for a d=1 channel code).

The finite state diagrams for the 3-taps and 5-taps PRML are shown in Figures 1 and 2, respectively. Figure 3 compares the performance in terms of bit-error-rate (BER) for a d=1 experiment for phase-change recording. The gain between 3-taps and 5-taps is due to differentiation for the short runlengths, i.e. I2 and I3. In the case of the 3-taps PRML, the first bits (or the last bits) of an I2 and an I3 are related to the same state; this implies that the same reference amplitude level is used upon computing the likelihood. In the case of the 5-taps PRML, the runs I2 and I3 follow separate paths through the finite state diagram so that the difference in amplitude level can be accounted for. For the 5-taps PRML, additional states are present in the finite state diagram which are related to the longer runs from I4 on; the 5-taps states $(-1)(1)^4$ and $(1)^4(-1)$ on the positive bit-side (+1), and the states $(1)^4(1)$ and $(1)(-1)^4$ on the negative bit-side (-1) are visited for the runs I4 and larger, the states $(1)^5$ and $(-1)^5$ are visited for the runs I5 and larger. For the 3-taps PRML, all the runs longer than I3 pass through the states $(1)^3$ or $(-1)^3$.

The gain between 3-taps and 5-taps is not due to the differentiation on the amplitude levels for the outer bits of the longer runlengths In ($n \geq 3$) so that the states $(-1)(1)^4$, $(1)^4(-1)$, $(1)^5$ and $(-1)(1)^3(-1)$ can be merged into a joint state $b_1(1)^3b_5$, with the first bit b_1 and the fifth bit b_5 can be either +1 or -1. The inner bits of a run are defined as all the bits in the run, except the two outer bits. In other words, for the inner bits of the longer runs (from I4 on), a 3-taps PRML might be sufficient. The merging of the 4 states into a single one (at both bit-sign sides) yields a reduced complexity in the finite state diagram, as shown in Figure 4. The number of states now equals 10 instead of 16, as listed in Table 1. The performance of the 5-taps-r.c. (reduced complexity) detector is shown in Figure 5; the performance loss compared to the full-fledged 5-taps detector is relatively small.

The main advantage of the 5-taps reduced complexity PRML is that it yields only a 67% increase in complexity compared to a 3-taps PRML, whereas the full-fledged 5-taps PRML requires an increase of 167% in complexity.

The amplitude levels retrieved in a phase-change optical recording experiment as a function of tangential tilt, are shown in Figure 6 for a 5-taps PRML, using the linear averaging process described in the earlier filed EP patent application no. 98203146.0. The reduction in states for the 5-taps reduced complexity PRML consists in reducing the 4 upper and 4 lower levels into only two separate levels (actually, the ones with lowest absolute value

of the amplitude). Those are the levels of the states 1^5, $1^4(-1)$, $(-1)1^4$ and $(-1)1^3(-1)$ in figure 2, identified in figure 4 by the state $b_1 1^3 b_5$, and the levels of the states $(-1)^5$, $1(-1)^4$, $(-1)^4 1$ and $1(-1)^3 1$ in figure 2, identified by the state $b_1(-1)^3 b_5$ in figure 4. The levels corresponding with the shorter runs I2, via the states $(-1)1^2(-1)^2$ and $(-1)^2 1^2(-1)$ in figures 2 and 4, and I3, via the states $1^3(-1)^2$ and $(-1)^2 1^3$ in figures 2 and 4, are left intact.

Next, a description will be given of the functioning of a 'bit recursive' PRML detector. For simplicity reasons, in the following description it will be assumed that the window introduced below is (n=) 3 bits long. In accordance with the invention, however, n should be larger than 3, otherwise the basic principle of combining states is not applicable.

Figure 7 shows a signal waveform a(t) from which a sequence of bits should be detected by a PRML detector. The signal waveform can be an analog input information signal or an oversampled digital signal. The signal waveform is sampled at sampling instants, given by the instants ..., t_{i-2}, t_{i-1}, t_i, t_{i+1}, t_{i+2}, ... in figure 7. The sampling instants are 'bit synchronous' or have a phase difference of 180° with respect to the bit locations in the signal. Windows ...., w_{i-1}, w_i, w_{i+1}, ... are shown indicating the subsequent n(=3, in the present example)-sample sequences that correspond to states of the finite state diagram of figure 1, in the present example. Those states are given by ...., $s(t_{i-1})$, $s(t_i)$, $s(t_{i+1})$, ... in figure 7. The states correspond to 3-bit bitsequences b_{i-2}, b_{i-1}, b_i for the window w_{i-1}, b_{i-1}, b_i, b_{i+1} for the window w_i, and b_i, b_{i+1}, b_{i+2} for the window w_{i+1}, as shown in figure 7. Whilst for d=0, the number of possible states is 8, for d=1, the number of possible states is 6, as shown in figure 1.

Partial response detection on the sequence of samples shown in figure 7 is realized in the following way. Figure 8 shows again the state transition diagram of figure 1 for the 3-taps partial response with d=1. Figure 8 further shows the trellis diagram corresponding to the said response. The trellis diagram shows the transitions between the possible states for subsequent time instants t_{i-1} and t_i.

PRML bit-detection in a Viterbi detector is based on finding the best path, back in time, through the trellis diagrams repeatedly for direct preceding time instants. This best path leads to a state at the time instant t_{i-N}, which state corresponds to a detected bit at said time instant t_{i-N} and thereby yields a detected bit at said time instant t_{i-N}. Normally, the central bit of the n bit sequence related to that state is taken to be the detected bit.

In the foregoing it is assumed that the sampling frequency substantially equals the bit frequency in the information signal. In some situations, it may be possible to subsample the information signal, eg. by a factor of two. Now, the 'back tracking' algorithm is performed

at the pace of two bits. Now, the state at the time instant t_{i-N} yields two detected bits at said time instant t_{i-N}.

The derivation of the best path can be realized by carrying out the following calculations. Assume that a path-cost or path-metric value $PM(s_j,t_{i-1})$ is known for each of the states s_j, at the time instant t_{i-1}, where j runs from 1 to 6 in figure 8. Further, assume that a best predecessor state $PS(s_j,t_{i-1})$ is available for each of the states s_j at the time instant t_{i-1}. Now, a path-cost or path-metric $PM(s_j,t_i)$ can be calculated for each of the states s_j, at the time instant t_i, where j again runs from 1 to 6, in the following way:

For the transition from time instant t_{i-1} to time instant t_i, a branch metric value $BM[s_j(t_{i-1}),s_k(t_i)]$ for each of the states s(k) at the time instant t_i is computed. That means that, in the example of figure 8, the following branch metric values are calculated: $BM[s_1(t_{i-1}),s_5(t_i)]$, $BM[s_1(t_{i-1}),s_6(t_i)]$, $BM[s_2(t_{i-1}),s_1(t_i)]$, $BM[s_3(t_{i-1}),s_2(t_i)]$, $BM[s_3(t_{i-1}),s_3(t_i)]$, $BM[s_4(t_{i-1}),s_2(t_i)]$, $BM[s_4(t_{i-1}),s_3(t_i)]$, $BM[s_5(t_{i-1}),s_4(t_i)]$, $BM[s_6(t_{i-1}),s_5(t_i)]$ and $BM[s_6(t_{i-1}),s_6(t_i)]$.

More specifically, the branch metric value $BM[s_j(t_{i-1}),s_i(t_i)]$ can in the present example be calculated by means of one of the following formulas:

$$BM[s_j(t_{i-1}),s_k(t_i)] = \{a_i - A(s_k)\}^2$$

or

$$BM[s_j(t_{i-1}),s_k(t_i)] = |a_i - A(s_k)|,$$

where a_i is the sample value at the time instant t_i and $A(s_k)$ is the amplitude value corresponding to the state s_k. The derivation of the amplitude values $A(s_k)$ has been extensively described in earlier filed EP patent application no. 98203146.0. For the structure of the finite state machine considered here, and as one can see from the above formula, the branch metric value $BM[s_j(t_{i-1}),s_k(t_i)]$ is independent of the state s_j at the time instant t_{i-1}.

The six path metric values $PM(s_1,t_i)$ to $PM(s_6,t_i)$ can now be obtained in the following way.

- $PM(s_1,t_i) = PM(s_2,t_{i-1}) + BM[s_2(t_{i-1}),s_1(t_i)]$. Further, the best predecessor state for state s_1 is (always) the state s_2.
- $PM(s_4,t_i) = PM(s_5,t_{i-1}) + BM[s_4(t_{i-1}),s_5(t_i)]$. Further, the best predecessor state for state s_4 is (always) the state s_5.

- two path metric values can be derived for state s_2, namely a first one defined as

$PM^1(s_2,t_i) = PM(s_3,t_{i-1}) + BM[s_3(t_{i-1}),s_2(t_i)]$, and the second one defined as

$PM^2(s_2,t_i) = PM(s_4,t_{i-1}) + BM[s_4(t_{i-1}),s_2(t_i)]$.

The two path metric values $PM^1(s_2,t_i)$ and $PM^2(s_2,t_i)$ are compared to each other and the smallest is chosen as the actual path metric value. Suppose this is $PM^2(s_2,t_i)$. Now, the best predecessor state for the state s_2 at the time instant t_i is the state s_4.

- two path metric values can be derived for state s_3, namely a first one defined as

$PM^1(s_3,t_i) = PM(s_3,t_{i-1}) + BM[s_3(t_{i-1}),s_3(t_i)]$, and the second one defined as

$PM^2(s_3,t_i) = PM(s_4,t_{i-1}) + BM[s_4(t_{i-1}),s_3(t_i)]$.

The two path metric values $PM^1(s_3,t_i)$ and $PM^2(s_3,t_i)$ are compared to each other and the smallest is chosen as the actual path metric value. Suppose this is $PM^1(s_3,t_i)$. Now, the best predecessor state for the state s_3 at the time instant t_i is the state s_3.

- two path metric values can be derived for state s_5, namely a first one defined as

$PM^1(s_5,t_i) = PM(s_1,t_{i-1}) + BM[s_1(t_{i-1}),s_5(t_i)]$, and the second one defined as

$PM^2(s_5,t_i) = PM(s_6,t_{i-1}) + BM[s_6(t_{i-1}),s_5(t_i)]$.

The two path metric values $PM^1(s_5,t_i)$ and $PM^2(s_5,t_i)$ are compared to each other and the smallest is chosen as the actual path metric value. Suppose this is $PM^1(s_5,t_i)$. Now, the best predecessor state for the state s_5 at the time instant t_i is the state s_1.

- two path metric values can be derived for state s_6, namely a first one defined as

$PM^1(s_6,t_i) = PM(s_1,t_{i-1}) + BM[s_1(t_{i-1}),s_6(t_i)]$, and the second one defined as

$PM^2(s_6,t_i) = PM(s_6,t_{i-1}) + BM[s_6(t_{i-1}),s_6(t_i)]$.

The two path metric values $PM^1(s_6,t_i)$ and $PM^2(s_6,t_i)$ are compared to each other and the smallest is chosen as the actual path metric value. Suppose this is $PM^2(s_6,t_i)$. Now, the best predecessor state for the state s_6 at the time instant t_i is the state s_6.

The above described calculation is carried out each time for subsequent time instants.

Figure 9 shows the various possible paths through the states, for subsequent time instants. It will be assumed that the optimum state at the time instant t_0, is the state 1^3. This state will thus be the result of applying the 'back tracking algorithm' at the time instant t_i over N time instants, backwards in time, towards the time instant t_0, which is considered to be the starting point of the PRML algorithm. Suppose that the time interval between t_i and t_0 (that is the length of time covered by N time instants) is sufficiently long, so that the PRML detection can be considered to supply correctly detected bits. The first bit at the time instant t_0 can now be derived in the following way.

The smallest of the path metric values $PM(s_1,t_i)$ to $PM(s_6,t_i)$ is established. Suppose this is the path metric value $PM(s_4,t_i)$. Now, a back tracking operation is carried out in backwards direction in time, going out from the state s_4, at the time instant t_i, via its corresponding best predecessor state, which is the state s_5 at the time instant t_{i-1}. Using the best predecessor state for the state s_5 at the time instant t_{i-1}, a state at the time instant t_{i-2} can be found. This is continued until the time instant t_{i-N} has been reached, which is the time instant t_0, so as to enable the detection of the first bit. It will turn out that at the time instant t_0, the path leads to the state s_6, so that the first bit detected, bit b_1, is a '1' bit, see figure 9a.

The above processing is again carried out when having calculated all the path metric values $PM(s_1,t_{i+1})$ to $PM(s_6,t_{i+1})$. The back tracking operation described above will now lead to the state s_5 at the time instant t_2, so that the bit b_2 equals a '1' bit, see figure 9b.

The above processing is again carried out when having calculated all the path metric values $PM(s_1,t_{i+2})$ to $PM(s_6,t_{i+2})$. The back tracking operation described above will now lead to the state s_4 at the time instant t_3, so that the bit b_3 equals a '0' bit, see figure 9c.

In the above described derivation of the path metric values, especially those for the states s_2, s_3, s_5 and s_6, an 'add-compare-select' method is used, namely, first, the branch metric value and the path metric value are added. This is done twice for the states mentioned. Next, both resulting path metric values PM^1 and PM^2 are compared to each other in order to determine the smallest one. However, as has been stated above, the branch metric values only depend on the final state. Therefore, a compare-select-add operation can be carried out, resulting in yet another reduction in complexity of the algorithm. One could namely first compare the path metric values of the possible predecessor states at the time instant t_{i-1} (the states s_1 and s_6, when we are concerned with deriving the path metric value for the state s_5 at the time instant t_i), choose the smaller one and add the branch metric value to the path metric value chosen so as to obtain the path metric value for the state s_5.

Figure 10 shows the application of the invention in another embodiment. More specifically, figure 10a shows the finite state diagram for the 5-taps PRML where d equals 3. The state diagram shown in Figure 10a has ten states in total. In accordance with the invention, the reduction in states for the 5-taps reduced complexity PRML of figure 10a consists in reducing the 3 upper and 3 lower levels into only two separate levels (actually, the ones with lowest absolute value of the amplitude). This results in the finite state diagram of figure 10b. Those levels are the levels of the states 1^5, $1^4(-1)$ and $(-1)1^4$ in figure 10a, identified in figure 10b by the state $b_1 1^3 b_5$, and the levels of the states $(-1)^5$, $1(-1)^4$ and $(-1)^4 1$ in figure 10a, identified by the state $b_1(-1)^3 b_5$ in figure 10b.

Figure 11 shows the application of the invention in again another embodiment. More specifically, figure 11a shows the finite state diagram for the 7-taps PRML where d equals 3. The state diagram shown in Figure 11a has 20 states in total. Not all of them are shown. It will be understood that the portion of the finite state diagram to the left of the vertical broken line in figure 11a should be, more or less 'mirror imaged' along this line in order to obtain the portion of the finite state diagram to the right of that line.
In accordance with the invention, the reduction in states for the 7-taps reduced complexity PRML of figure 11a consists in reducing the 4 upper and 4 lower levels into only two separate levels (actually, the ones with lowest absolute value of the amplitude). This results in the finite state diagram of figure 11b. Those levels are the levels of the states 1^7, $1^6(-1)$, $(-1)1^6$ and $(-1)1^5(-1)$ in figure 11a, identified in figure 10b by the state $b_1 1^5 b_7$, and the corresponding levels of the states $(-1)^7$, $1(-1)^6$, $(-1)^6 1$ and $1(-1)^5 1$, not shown in figure 11a, which should be identified by a combined state $b_1(-1)^5 b_7$ in figure 11b.

Figure 12 shows an embodiment of the PRML detection apparatus in accordance with the invention. The apparatus has an input 120 for receiving the information signal, which is coupled to an input of a sampling unit 122. The sampling unit 122 samples the information signal with a sampling frequency f_s, resulting in sample values a_i at sampling instants t_i that are supplied to a calculation unit 124. The apparatus further comprises a memory unit 126 in which the reference amplitudes $A(s_k)$, one for each of the states s_k, are stored. The apparatus further comprises a memory unit 128 in which vectors are stored, one for each of the states, and one for a plurality of previous time instants. A vector for a state s_k at a time instant t_i is indicative of the best predecessor state for the said state at the directly preceding time instant t_{i-1}. The vectors of all possible states s_k at the time instant t_i are stored in a vertical column in the memory unit 128. Further, there are N columns in the memory unit 128.

The apparatus further comprises a path metric value memory unit 130, having as many storage locations as there are possible states s_k in the 'reduced complexity' finite state diagram. Each location has a path metric value stored for a state s_k at the time instant t_i. The memory unit 128 has a coupling to the calculation unit 124 via the connection 138. The memory unit 130 has a coupling to the calculation unit 124 via the connection 136. The memory unit 128 further has an output coupled to a state-to-bit converter unit 132, which has an output coupled to the output terminal 134 of the apparatus.

The functioning of the apparatus is as follows. Upon supplying a new sample value a_i by the sampling unit 122 to the calculation unit 124, the calculation unit 124 retrieves

the $A(s_k)$ values from the memory 126 and the calculation unit 124 calculates the branch metric values in the way as explained above. Next, the calculation unit 124 calculates the path metric values $PM(s_k,t_i)$ in the way as explained above. That is: one path metric value for each of the states s_k, using the path metric values $PM(s_k,t_{i-1})$ stored in the memory unit 130, for the previous time instant t_{i-1}. The path metric values $PM(s_k,t_i)$ obtained are stored in the memory unit 130, over the old path metric values, as the new path metric values for the time instant t_i. Further, vectors, one vector for each of the states s_k, are derived, indicating the best predecessor state at the time instant t_{i-1}. Upon shifting the contents in all the rows in the memory unit 128 over one position to the left, the most right column in the memory unit becomes available for receiving the vectors for the states s_k. Those vectors are supplied via the line 138 to the memory unit 128 and stored in the most right column.

The calculation unit further comprises a comparator (not shown) for comparing the path metric values $PM(s_k,t_i)$, to determine the smallest one. This leads to one of the states at the time instant t_i, which state is the first state in the 'back tracking algorithm', using the vectors stored in the memory 128. The 'back tracking algorithm' results in pointing to one of the states using a vector in the most left column of the memory 128. An indicator signal indicating said state is supplied to the converter unit 132, which generates a bit (or two bits) in response to the state selected.

The above algorithm is repeated for subsequent sample values supplied to the calculation unit 124, resulting in a sequence of bits at the output terminal 134.

Whilst the invention has been described with reference to preferred embodiments thereof, it is to be understood that these are not limitative examples. Thus, various modifications may become apparent to those skilled in the art, without departing from the scope of the invention, as defined by the claims. As an example, when comparing the figures 2 and 4, one sees that in the embodiment described, all states having three central '1's have been combined into one state and all states having three central '-1's have been combined into one state. However, one could have chosen otherwise, such as combining all states having four '1's in the 5-bit bit sequence into one state and combining all states having four '-1's into one state.

As a second example, when comparing the figures 11a and 11b, one sees that in the embodiment described, all states having five central '1's have been combined into one state and all states having five central '-1's have been combined into one state. However, one could have chosen otherwise, such as combining all states having six '1's in the 7-bit bit sequence into one state and combining all states having six '-1's into one state.

Further, any reference signs do not limit the scope of the claims. The invention can be implemented by means of both hardware and software, and several "means" may be represented by the same item of hardware. The word 'comprising' does not exclude the presence of other elements or steps than those listed in a claim. Also, the word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements. In addition, the invention lies in each and every novel feature or combination of features.

CLAIMS:

1. A partial response maximum likelihood (PRML) bit detection apparatus for deriving a bit sequence from an input information signal, comprising

- input means (1) for receiving the input information signal,
- sampling means for sampling, at a predetermined sampling frequency, the input information signal at sampling instants t_i so as to obtain sample values of the input information signal at said sampling instants t_i, said sampling frequency having a relationship with a bit frequency,
- calculation means for

(a) calculating at a sampling instant t_i for each of a plurality of states s_j at said sampling instant, an optimum path metric value $PM(s_j,t_i)$ and for determining for each of the plurality of states a best predecessor state at the directly preceding sampling instant t_{i-1}, a state at said sampling instant identifying a sequence of n subsequent bits,

(b) establishing the best path from the state at the said sampling instant t_i having the lowest optimum path metric value, back in time towards the sampling instant t_{i-N} via best predecessor states, established earlier for earlier sampling instants, to establish an optimum state at said sampling instant t_{i-N},

(c) outputting at least one bit of said n bits of the sequence of bits corresponding to said established optimum state at said sampling instant t_{i-N},

(d) repeating said steps (a) to (c) for a subsequent sampling instant t_{i+1},

characterized in that n is larger than 3, and that sequences of n subsequent bits having n-1 directly successive bits of the same binary value are allocated to the same state.

2. Apparatus as claimed in claim 1, wherein n is an even number, such as equal to 4.

3. Apparatus as claimed in claim 1, wherein n is an odd number larger than 4, and that sequences of n subsequent bits having n-2 directly successive bits of the same binary value as the central n-2 bits in such n-bit sequence, are allocated to the same state.

4. Apparatus as claimed in claim 3, wherein n=5.

5. Apparatus as claimed in claim 1, wherein said calculation means are adapted to obtain said optimum path metric value for a state by combining the optimum path metric value of the best predecessor state at said directly preceding sampling instant t_{i-1} and a branch metric value corresponding to said state, said branch metric value for said state being obtained from the sample value at said sampling instant and a reference amplitude, which reference amplitude has a relationship with said state.

6. A partial response maximum likelihood (PRML) bit detection apparatus for deriving a bit sequence from an input information signal, comprising

- input means (1) for receiving the input information signal,
- sampling means for sampling, at a predetermined sampling frequency, the input information signal at sampling instants t_i so as to obtain sample values of the input information signal at said sampling instants t_i, said sampling frequency having a relationship with a bit frequency,
- calculation means for

(a) calculating at a sampling instant t_i for each of a plurality of states s_j at said sampling instant, an optimum path metric value $PM(s_j,t_i)$ and for determining for each of the plurality of states a best predecessor state at the directly preceding sampling instant t_{i-1}, a state at said sampling instant identifying a sequence of n subsequent bits,

(b) establishing the best path from the state at the said sampling instant t_i having the lowest optimum path metric value, back in time towards the sampling instant t_{i-N} via best predecessor states, established earlier for earlier sampling instants, to establish an optimum state at said sampling instant t_{i-N},

(c) outputting at least one bit of said n bits of the sequence of bits corresponding to said established optimum state at said sampling instant t_{i-N},

repeating said steps (a) to (c) for a subsequent sampling instant t_{i+1},

characterized in that said calculation means is adapted to obtain said optimum path metric value for said state at said sampling instant t_i in step (a) by

(a1) comparing the optimum path metric values of all possible predecessor states at the directly preceding instant t_{i-1} of the said state at the instant t_i,

(a2) select the predecessor state at the directly preceding instant t_{i-1} having the smallest optimum path metric value as said best predecessor state,

(a3) combining the optimum path metric value of the best predecessor state at said directly preceding sampling instant t_{i-1} and a branch metric value corresponding to said state at said instant t_i, so as to obtain said optimum path metric value for said state, said branch metric value for said state being obtained from the sample value at said sampling instant and a reference amplitude, which reference amplitude has a relationship with said state.

7. Apparatus as claimed in claim 6, characterized in that n is larger than 3, and that sequences of n subsequent bits having n-1 directly successive bits of the same binary value are allocated to the same state.

8. Method of carrying out a partial response maximum likelihood (PRML) bit detection in the apparatus as claimed in claim 1 or 6.

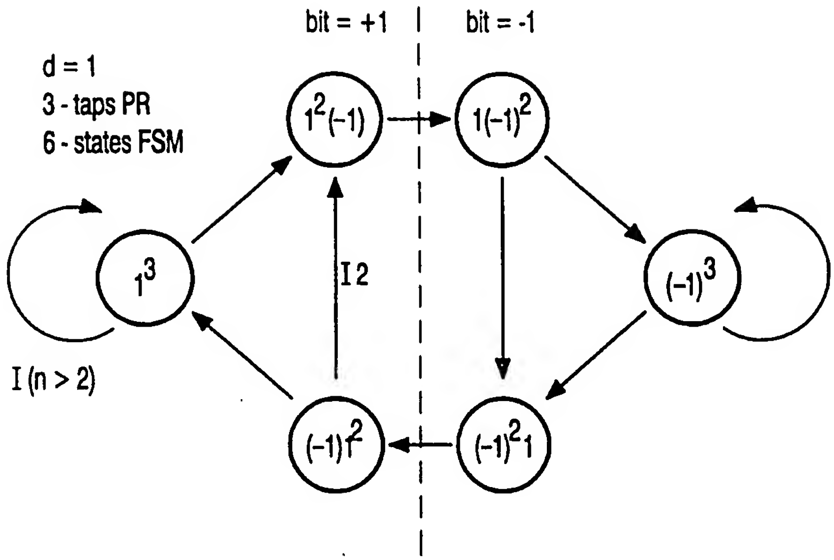
bit = +1
bit = -1
d = 1
3 - taps PR
6 - states FSM
$1^2(-1)$
$1(-1)^2$
1^3
$(-1)^3$
I 2
I (n > 2)
$(-1)1^2$
$(-1)^2 1$

FIG. 1

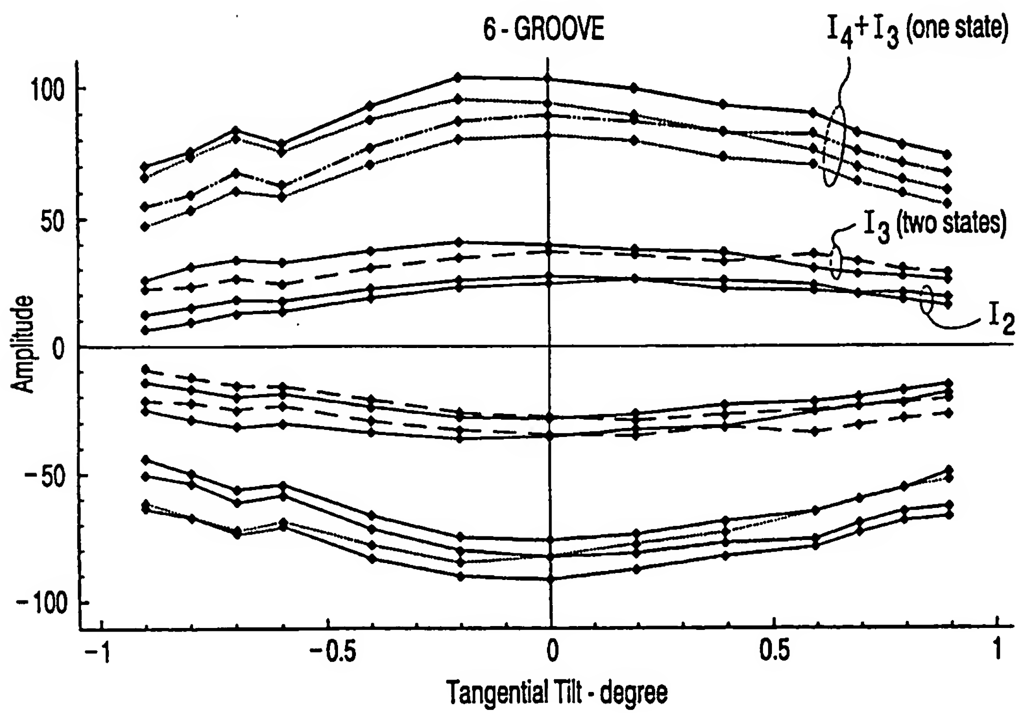
6 - GROOVE
$I_4 + I_3$ (one state)
I_3 (two states)
I_2
Amplitude
100
50
0
-50
-100
-1
-0.5
0
0.5
1
Tangential Tilt - degree

FIG. 6

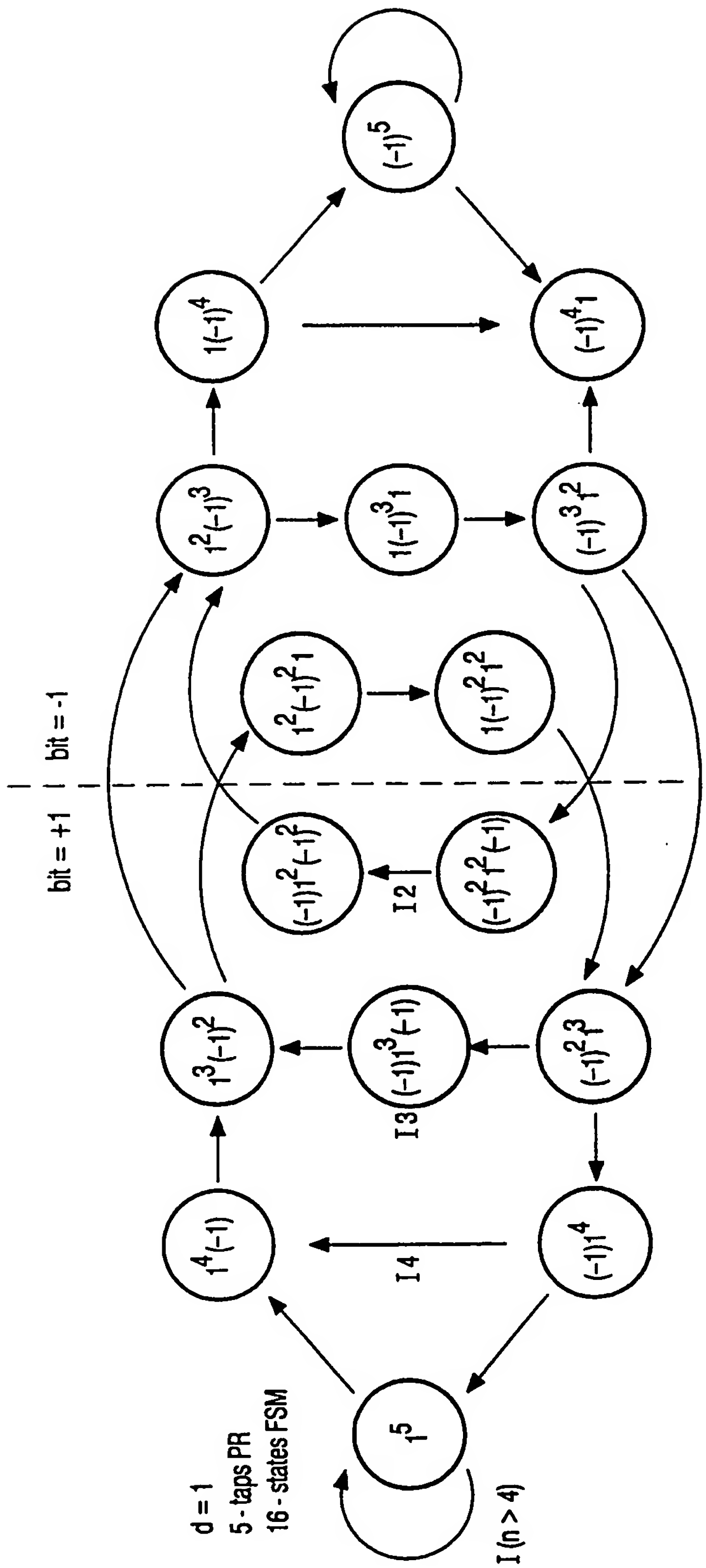

FIG. 2

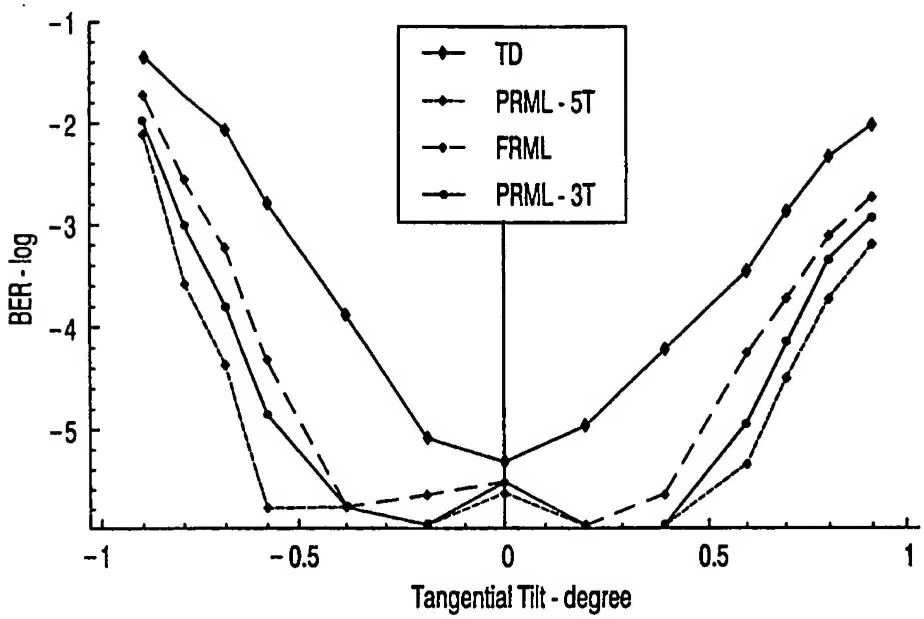
TD
PRML - 5T
FRML
PRML - 3T
BER - log
Tangential Tilt - degree
-1
-2
-3
-4
-5
-1
-0.5
0
0.5
1

FIG. 3

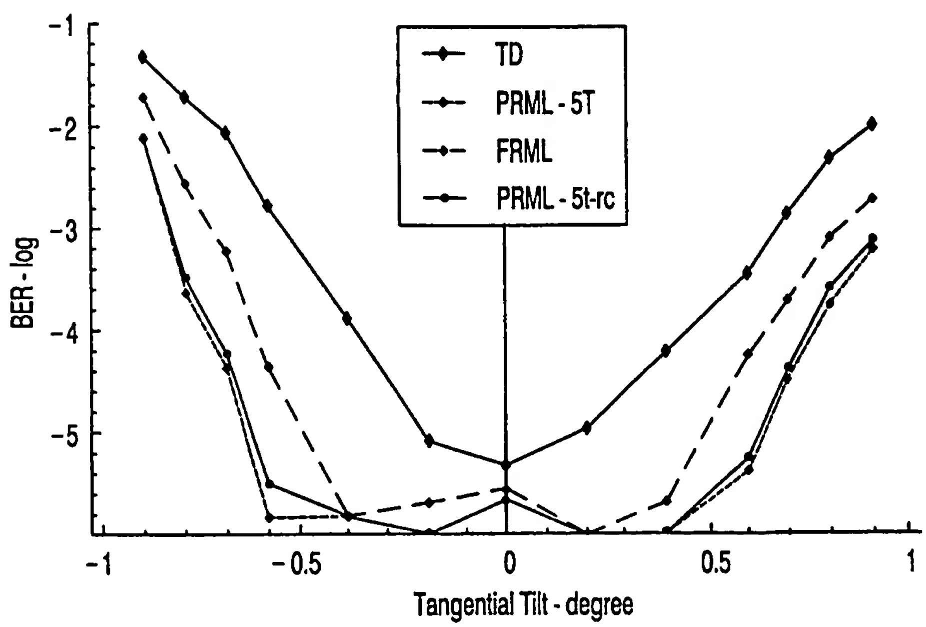
TD
PRML - 5T
FRML
PRML - 5t-rc
BER - log
Tangential Tilt - degree
-1
-2
-3
-4
-5
-1
-0.5
0
0.5
1

FIG. 5

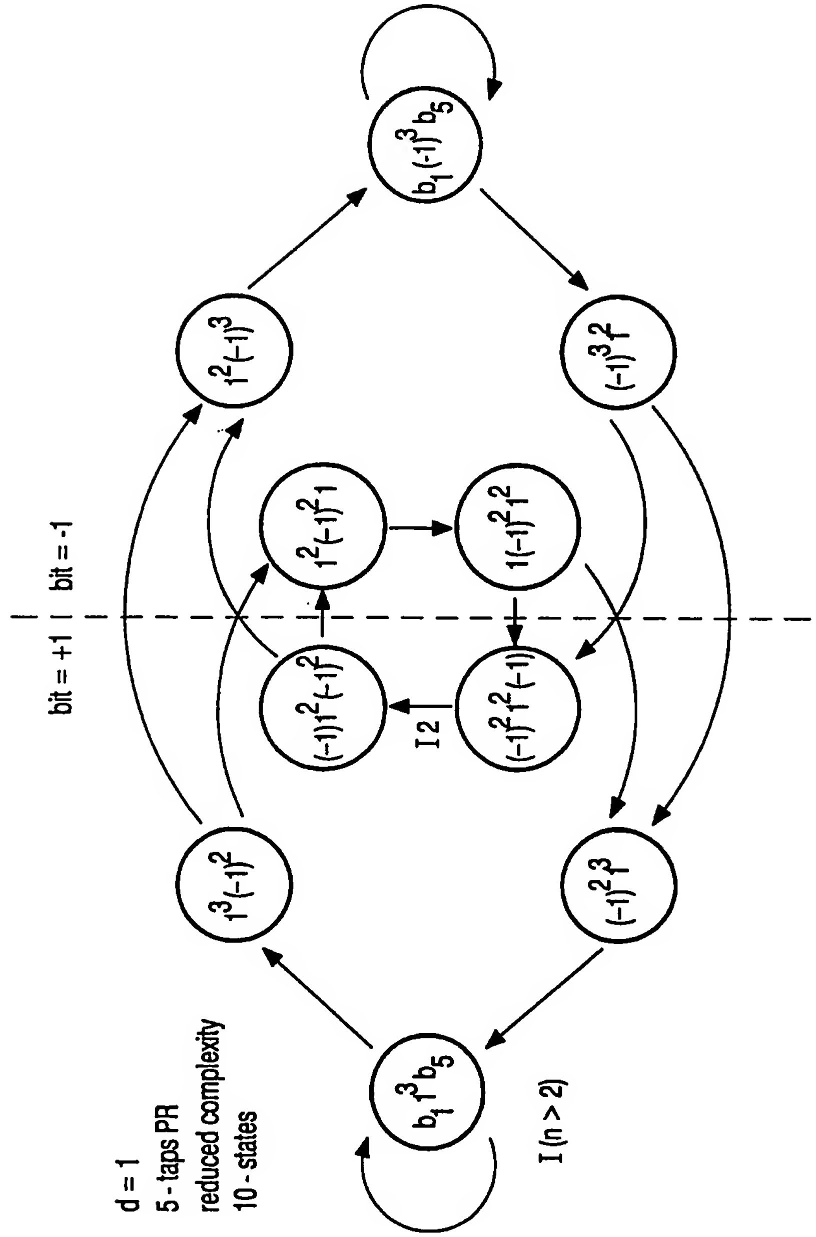

FIG. 4

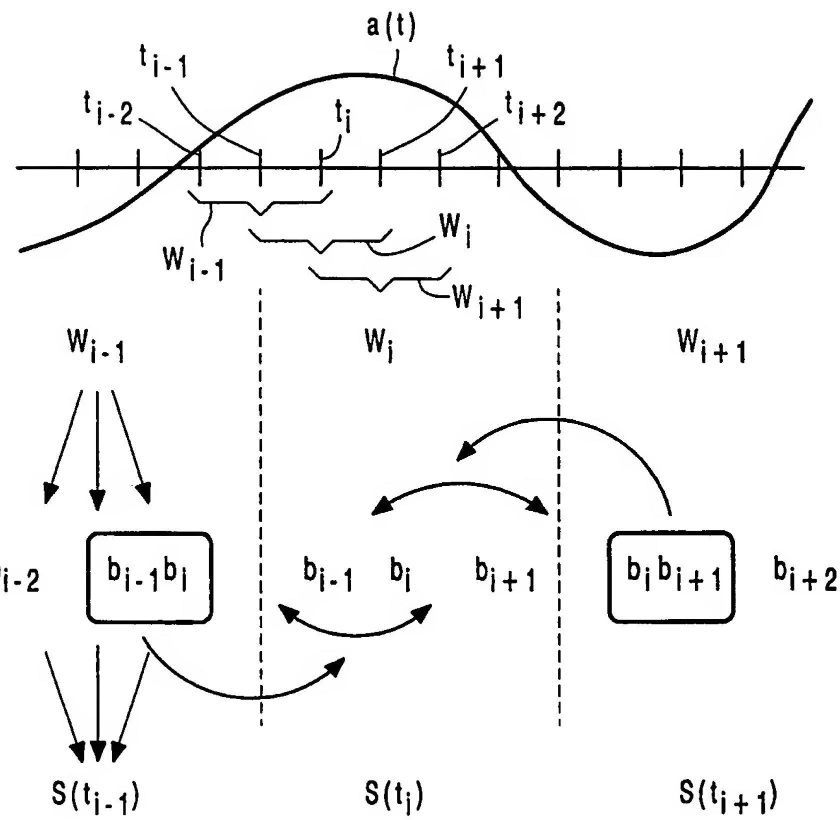
a(t)
t_{i-1}
t_{i+1}
t_{i-2}
t_i
t_{i+2}
W_i
W_{i-1}
W_{i+1}
W_{i-1}
W_i
W_{i+1}
b_{i-2}
$b_{i-1}b_i$
b_{i-1}
b_i
b_{i+1}
$b_i b_{i+1}$
b_{i+2}
$S(t_{i-1})$
$S(t_i)$
$S(t_{i+1})$

FIG. 7

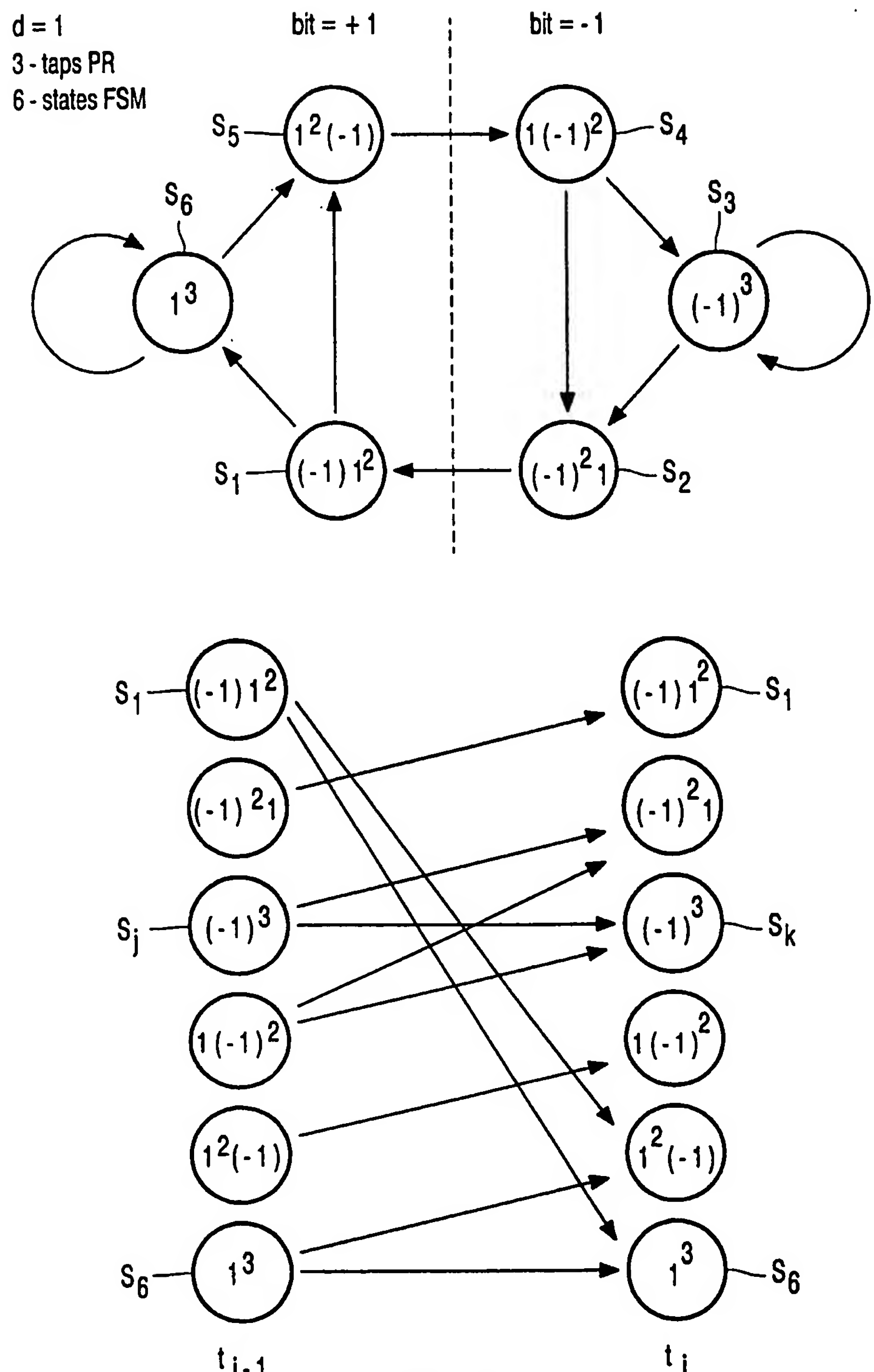
d = 1
3 - taps PR
6 - states FSM
bit = + 1
bit = - 1
S5
1²(-1)
1(-1)²
S4
S6
S3
1³
(-1)³
S1
(-1)1²
(-1)²1
S2
S1
(-1)1²
(-1)²1
Sj
(-1)³
Sk
1(-1)²
1²(-1)
S6
1³
t i-1
t i

FIG. 8

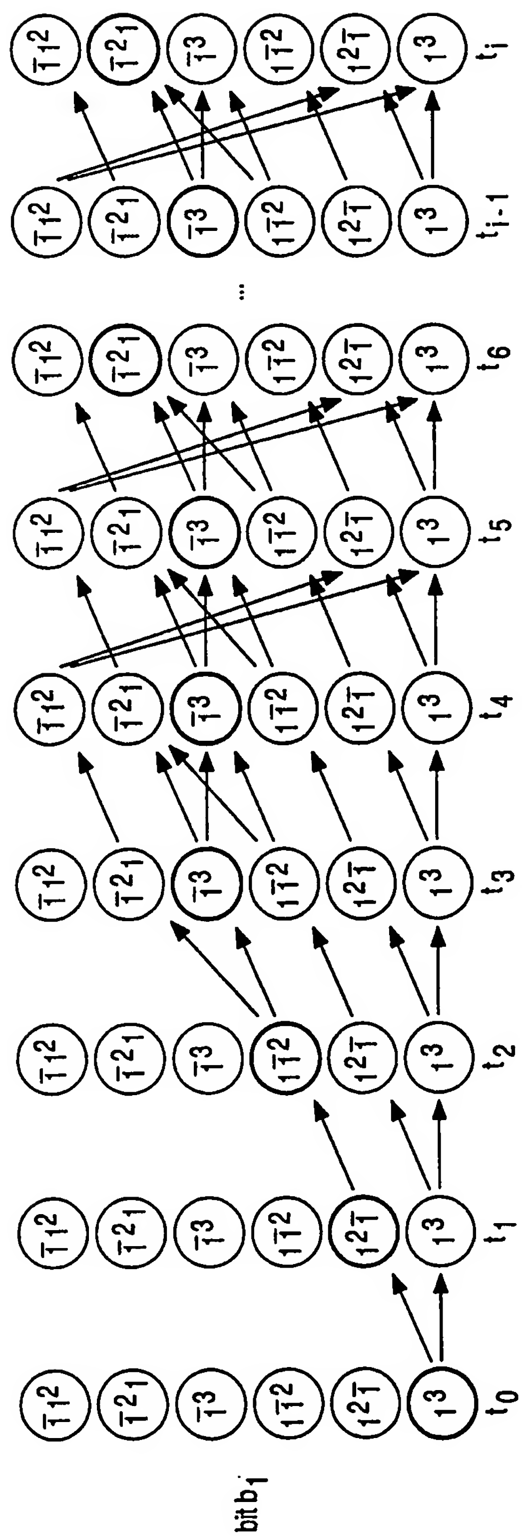

FIG. 9a

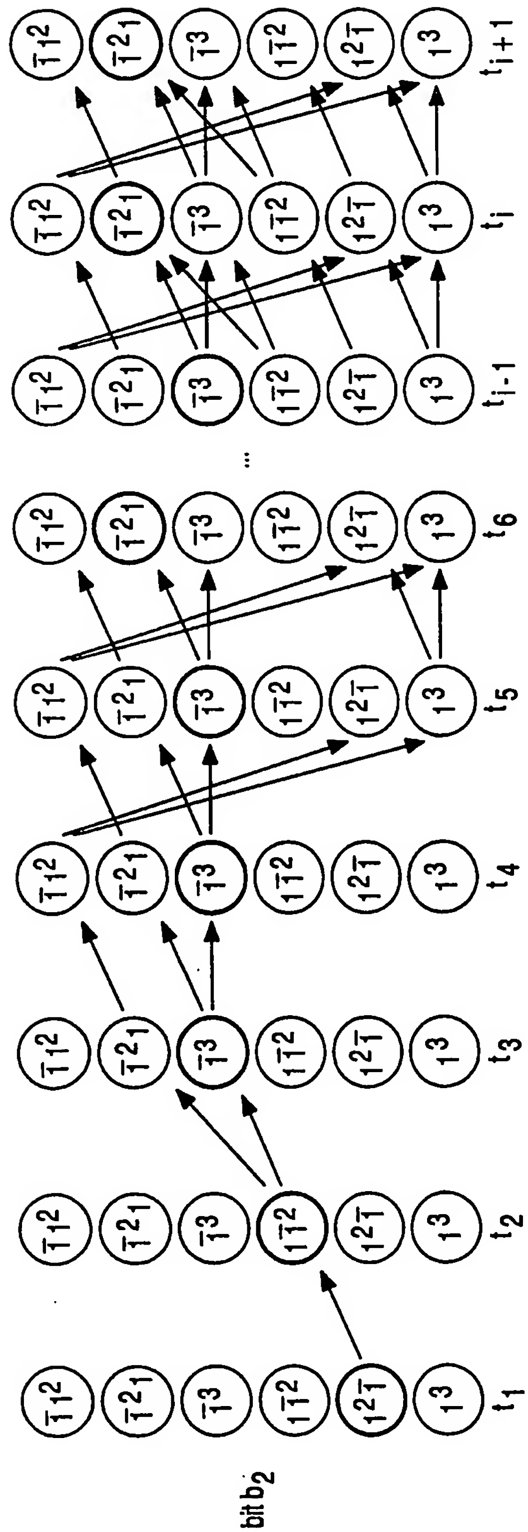

FIG. 9b

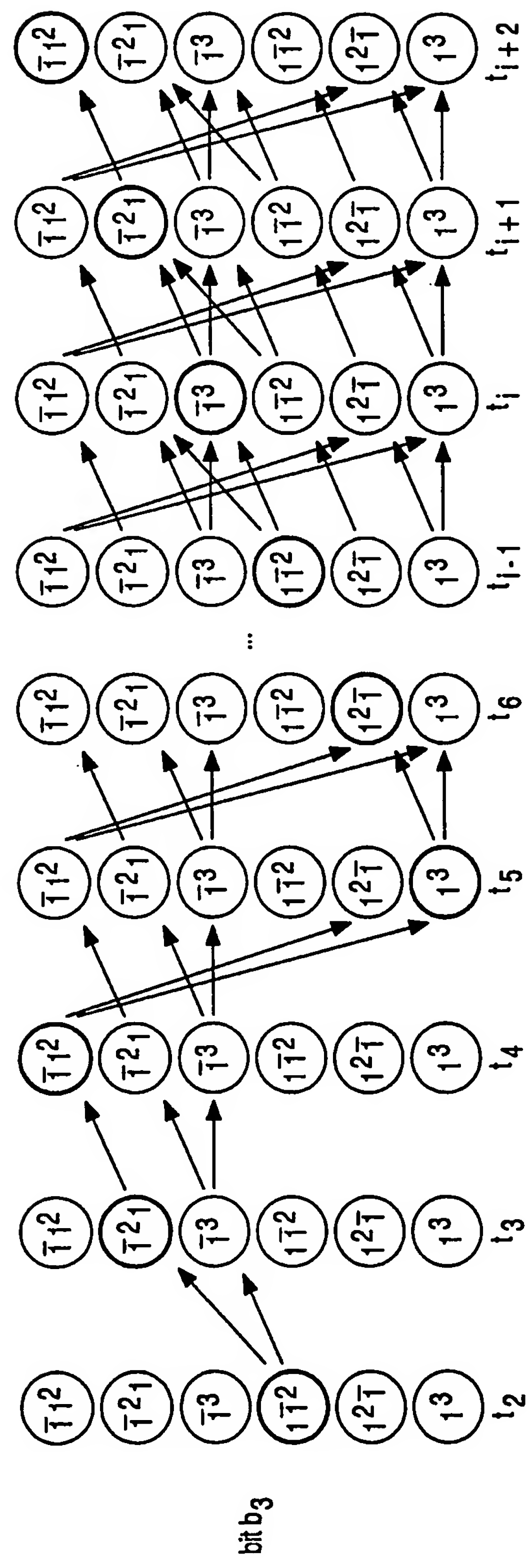

FIG. 9c

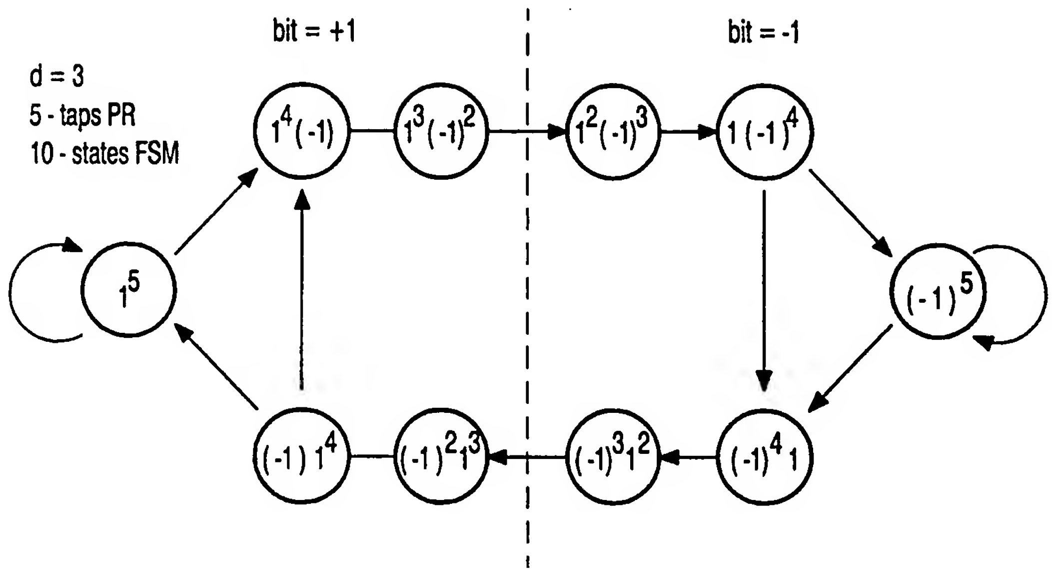

FIG. 10a

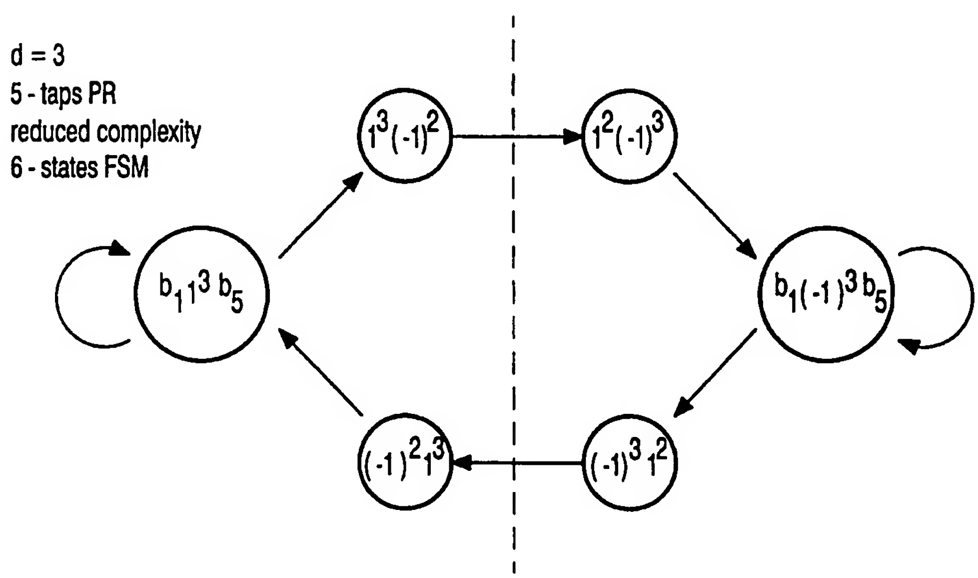

FIG. 10b

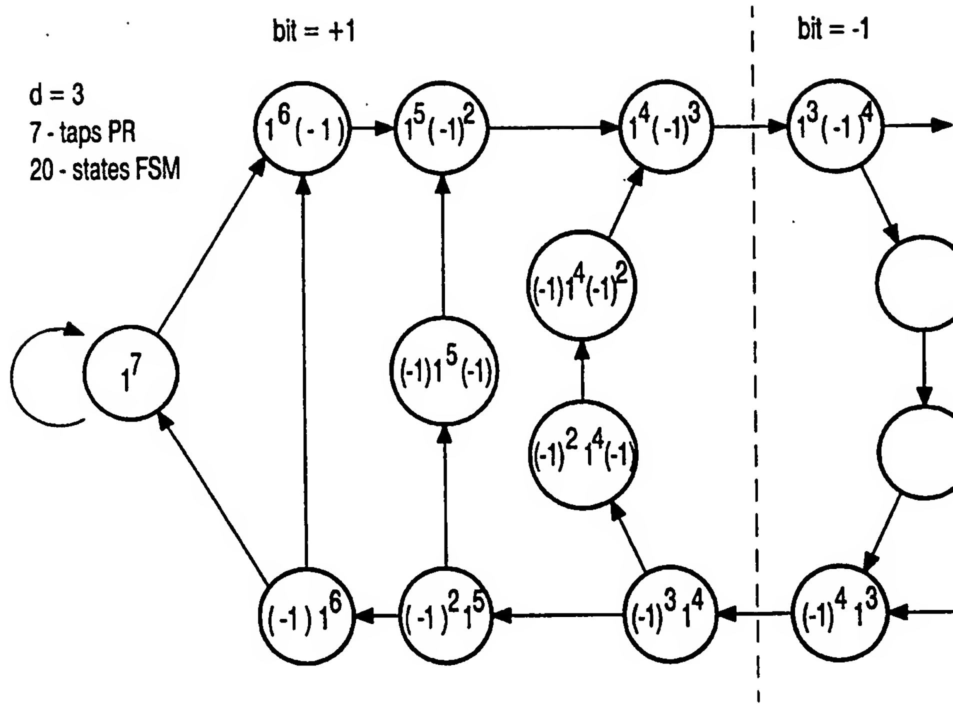

FIG. 11a

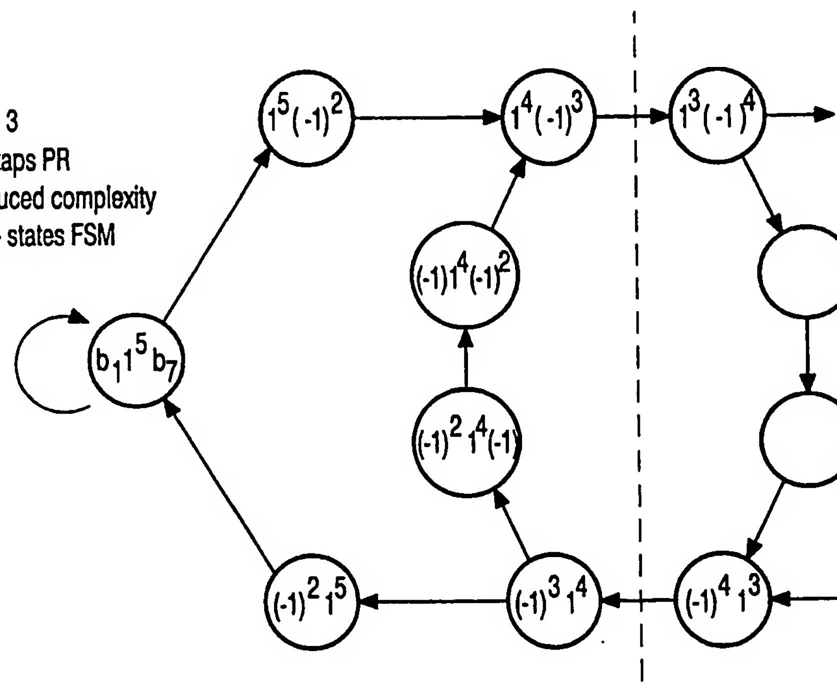

FIG. 11b

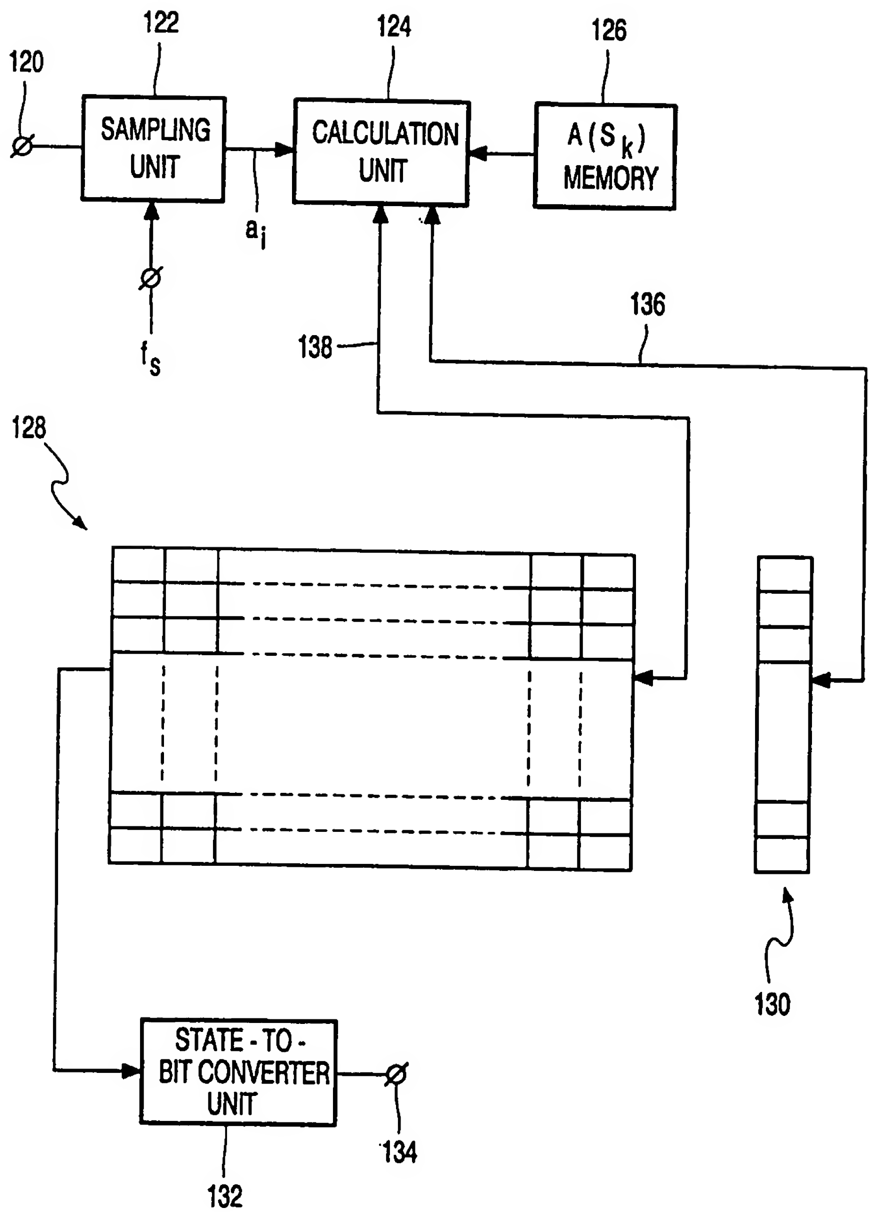
120
122
SAMPLING UNIT
124
CALCULATION UNIT
126
A (S_k) MEMORY
a_i
f_S
136
138
128
130
STATE - TO - BIT CONVERTER UNIT
134
132

FIG. 12

INTERNATIONAL SEARCH REPORT

Int tional Application No
PCT/EP 99/06570

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03M13/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11B H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 647 036 A (IBM) 5 April 1995 (1995-04-05)	6,8
Y	page 4, line 23 -page 4, line 35 page 7, line 13 -page 8, line 14; figure 5	1-5,7
Y	B.H. MARCUS, P.H. SIEGEL & J.K. WOLF: "Finite-State Modulation Codes for Data Storage" IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS, vol. 10, no. 1, January 1992 (1992-01), pages 5-37, XP000462064 New York page 19, column 2, line 25 -page 22, column 1, line 18; figure 18	1-5,7

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 December 1999	12/01/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Van Staveren, M

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 99/06570

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 291 499 A (CIRRUS LOGIC) 1 March 1994 (1994-03-01) abstract -----	1,6,7

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP 99/06570

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 647036 A	05-04-1995	US 5430744 A	04-07-1995
		JP 2755375 B	20-05-1998
		JP 7183819 A	21-07-1995
		SG 43743 A	14-11-1997
US 5291499 A	01-03-1994	AU 3918193 A	21-10-1993
		EP 0663085 A	19-07-1995
		JP 7507187 T	03-08-1995
		SG 46527 A	20-02-1998
		WO 9319418 A	30-09-1993